CLAIMS

1. An array architecture for a memory device, comprising a memory cell block comprising an even number of memory cells and a transistor, wherein said memory cells are electrically coupled to said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor.

2. The array architecture of claim 1, wherein a first half of said memory cells of said memory cell block is electrically coupled to the first side of said transistor and a second half of said memory cells is electrically coupled to the second side of said transistor such that said first half of said memory cells are electrically coupled to said second half of said memory cells via said transistor when said transistor is activated.

3. The array architecture of claim 1, wherein each memory cell is in electrical communication with a respective bit line.

4. The array architecture of claim 3, wherein each bit line is in electrical communication with a sensing circuit.

5. The array architecture of claim 3, wherein upon addressing a first memory cell of said memory cell block a sneak path includes any second memory cell of said memory cell block that is electrically coupled to a same side of said transistor as said first memory cell and any third memory cell electrically coupled to a same bit line as said first and second memory cells.

6. The array architecture of claim 3, wherein a gate of said transistor is electrically coupled to a wordline.

7. The array architecture of claim 6, wherein a sneak path resistance is $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$, where R is a combined resistance of each memory cell of said sneak path, n is a number of memory cells of said memory cell block electrically coupled to a same side of said transistor as an addressed memory cell, and m is a total number of wordlines of the array architecture.

8. The array architecture of claim 1, wherein at least two memory cells are electrically coupled to each side of said transistor.

9. The array architecture of claim 1, wherein said memory cells are non-volatile.

10. The array architecture of claim 1, wherein said memory cells are semi-volatile.

11. The array architecture of claim 1, wherein said memory cells comprise variable resistance memory elements.

12. The array architecture of claim 1, wherein said memory cells comprise MRAM memory elements.

13. The array architecture of claim 1, wherein said memory cells comprise PCRAM memory elements.

14. The array architecture of claim 1, wherein said memory cells comprise polymer memory elements.

15. The array circuit of claim 1, wherein said memory cells comprise phase-changing chalcogenide-based memory elements.

16. The array circuit of claim 1, wherein an equal number of said memory cells are coupled to each side of said transistor.

17. A memory device comprising:

at least a first memory cell;

at least a second memory cell; and

a gate electrode electrically coupling said first memory cell to said second memory cell, wherein said first memory cell is addressed for reading through said second memory cell and said gate electrode.

18. The memory device of claim 17, further comprising:

a first bit line in electrical communication with said first memory cell;

a second bit line in electrical communication with said second memory cell; and

a wordline in electrical communication with said gate electrode.

19. The memory device of claim 18, wherein said first and second bit lines and said wordline are included in a read circuit.

20. The memory device of claim 19, wherein said read circuit is generated upon grounding of said first bit line, forcing current on said second bit line, and applying voltage to said wordline.

21. The memory device of claim 20, wherein said first bit line is in electrical communication with a sensing circuit.

22. The memory device of claim 21, wherein a sneak path resistance for said read circuit is $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$; where R is a combined resistance of each said memory cell, n is a number of first memory cells, and m is a total number of wordlines of an array of the memory device.

23. The memory device of claim 17, comprising at least two first memory cells and at least two second memory cells.

24. The memory device of claim 17, wherein said first and second memory cells are PCRAM cells.

25. The memory device of claim 17, wherein said first and second memory cells are MRAM cells.

26. The memory device of claim 17, wherein said first and second memory cells are polymer memory cells.

27. The memory device of claim 17, wherein said first and second memory cells are phase-changing chalcogenide-based memory cells.

28. A processor system, comprising:

a processor; and

a memory circuit, comprising a memory cell block having a plurality of memory cells and a transistor, wherein said memory cells are electrically coupled to said transistor such that at least one of the memory cells is on a first side of said transistor and at least one other memory cell is on a second side of said transistor.

29. The processor system of claim 28, wherein a first half of said memory cells of said memory cell block is electrically coupled to the first side of said transistor and a second half of said memory cells is electrically coupled to the second side of said transistor such that said first half of said memory cells are electrically coupled to said second half of said memory cells via said transistor when said transistor is activated.

30. The processor system of claim 28, wherein each memory cell is in electrical communication with a respective bit line.

31. The processor system of claim 30, wherein each bit line is in electrical communication with a sensing circuit.

32. The processor system of claim 30, wherein upon addressing a first memory cell of said memory cell block a sneak path includes any second memory cell of said memory cell block that is electrically coupled to a same side of said transistor as said first memory cell and any third memory cell electrically coupled to a same bit line as said first and second memory cells.

33. The processor system of claim 30, wherein said transistor is in electrical communication with a wordline.

34. The processor system of claim 33, wherein a sneak path resistance is $[R/(n\text{-}1)] + [R/(m(n\text{-}1))]$, where R is a combined resistance of each said memory cell, n is a number of memory cells of said memory cell block electrically coupled to a same side of said transistor as an addressed memory cell, and m is a total number of wordlines of an array of the memory circuit.

35. The processor system of claim 28, wherein at least two memory cells are electrically coupled to each of said two sides of said transistor.

36. The processor system of claim 28, wherein said memory cells are non-volatile.

37. The processor system of claim 28, wherein said memory cells are semi-volatile.

38. The processor system of claim 28, wherein said memory cells comprise variable resistance memory elements.

39. The processor system of claim 28, wherein said memory cells comprise MRAM memory elements.

40. The processor system of claim 28, wherein said memory cells comprise PCRAM memory elements.

41. The processor system of claim 28, wherein said memory cells comprise polymer memory elements.

42. The processor system of claim 28, wherein said memory cells comprise phase-changing chalcogenide-based memory elements.

43. The processor system of claim 28, wherein an equal number of said memory cells are coupled to said first and said second sides of the transistor.

44. A method of reading stored data, comprising:

forming an electrical circuit between an addressed memory cell and a second memory cell, said circuit comprising a transistor gate electrically coupling said addressed memory cell to said second memory cell; and

sensing a resistance state of the addressed cell through the circuit.

45. The method of claim 44, wherein said addressed memory cell is in electrical communication with a first bit line, said second memory cell is in electrical communication with a second bit line, and said transistor is in electrical communication with a wordline, said first bit line being in electrical communication with a sensing circuit.

46. The method of claim 44, further comprising electrically coupling at least one third memory cell and at least one fourth memory cell to each other through said transistor when said transistor is activated.

47. The method of claim 46, wherein said third memory cell is in electrical communication with a third bit line and said fourth memory cell is in electrical communication with a fourth bit line.

48. The method of claim 44, wherein said addressed memory cell and said second memory cell comprise MRAM memory elements.

49. The method of claim 44, wherein said addressed memory cell and said second memory cell comprise PCRAM memory elements.

50. The method of claim 44, wherein said addressed memory cell and said second memory cell comprise polymer memory elements.

51. The method of claim 44, wherein said addressed memory cell and said second memory cell comprise phase-changing chalcogenide based memory elements.

52. The method of claim 44, wherein there are an equal number of said memory cells on a first side and a second side of said transistor gate.

53. The method of claim 44, further comprising calculating a sneak path resistance for said read circuit as $[R/(n\text{-}1) + [R/(m(n\text{-}1))]$, where R is a combined resistance of each memory cell of said read circuit, n is a number of memory cells electrically coupled to said transistor at a same side as said addressed memory cell, and m is a total number of wordlines.